IN THE CLAIMS:

Please CANCEL without prejudice or disclaimer claims 1-8 in the underlying PCT application and ADD new claims 9-16 in accordance with the following:

11 ~~9.~~ (new) A configuration for digital-analog conversion of a high-frequency digital input signal into a carrier-frequency analog output signal, comprising:

a delay device having at least one delay element, each delay element having an input and an output, the input of a first delay element receiving the high-frequency digital input signal and any additional delay elements connected downstream from the first delay element in a serially consecutive manner;

a first D/A converter having an input receiving the high-frequency digital input signal; and

at least one subsequent D/A converter, each having an input connected to the output of a corresponding delay element, all D/A converters controlled with an identical clock signal and having outputs combined in a step-by-step manner to form the analog output signal, where a filter characteristic is realized by assigning specific coefficients to the first and at least one subsequent D/A converters, respectively, and a specific delay time to each delay element, for a total delay time corresponding to at least part of a clock period of the identical clock signal such that the filter characteristic is automatically adjusted if there is a change in carrier frequency range of the output signal.

12 ~~10.~~ (new) A configuration according to claim 11 ~~9~~, wherein the specific coefficients and the specific delay time of each delay element are selected to realize a Finite Impulse Response filter characteristic.

13 ~~11.~~ (new) A configuration according to claim 12 ~~10~~, wherein each delay element is configured as a D latch timed with the identical clock signal.

14 ~~12.~~ (new) A configuration according to claim 13 ~~11~~, wherein all D/A converters are configured as 1-bit D/A converters.

15 ~~13.~~ (new) A configuration according to claim 14 ~~12~~, further comprising adding devices connected to the outputs of all D/A converters for combining thereof.

16 ~~14~~. (new) A configuration according to claim 15 ~~13~~, wherein the specific delay time assigned to each delay element is identical.

17 ~~15~~. (new) A configuration according to claim 16 ~~14~~, wherein each of the outputs of all D/A converters has a multiple pulse sequence, thereby improving the filter function.

18 ~~16~~. (new) A configuration according to claim 17 ~~15~~, wherein the high-frequency digital input signal is broadband.